PENDING CLAIM AND STATUS THEREOF

1. (previously amended) A system for prewriting a video frame in a liquid crystal display, said system comprising:

a liquid crystal display (LCD) having a matrix of liquid crystal pixels, said matrix further divided into a plurality of sub-matrices of pixels;

at least one digital-to-analog converter (DAC) adapted to receive a digital input representative of an analog voltage and having an analog output adapted for applying the analog voltage to at least one of the pixels at a time;

a plurality of column switches adapted for coupling the analog output of said at least one DAC to at least one of a plurality of columns of said LCD;

a plurality of row switches adapted for selectively coupling the plurality of columns to the pixels of said LCD;

logic circuits for calculating an average voltage value for each of the plurality of sub-matrices from final voltage values associated with the pixels of each of the sub-matrices; and

logic circuits for controlling the plurality of column switches and the plurality of row switches so that each sub-matrix may be precharged with its calculated average voltage value, then each of the pixels charged with the final voltage value representative of that portion of the video frame represented by that pixel.

2. (original) The system of claim 1, wherein the matrix of liquid crystals is K by L, where K and L are positive integer values.

3. (original) The system of claim 2, wherein $K > L$.

4. (original) The system of claim 2, wherein K = L.

5. (original) The system of claim 2, wherein K < L.

6. (original) The system of claim 2, wherein each of the sub-matrices is M by N, wherein M and N are positive integer values, K is greater than or equal to M and L is greater than or equal to N.

7. (original) The system of claim 6, wherein M is equal to N.

8. (original) The system of claim 6, wherein M is greater than N.

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9. (original) The system of claim 6, wherein M is less than N.

10. (original) The system of claim 2, wherein each of the sub-matrices is M by N, where M and N are positive integer values, and K is greater than or equal to M.

11. (original) The system of claim 2, wherein each of the sub-matrices is M by N, where M and N are positive integer values, and L is greater than or equal to N.

12. (original) The system of claim 7, wherein M = N = 8.

13. (original) The system of claim 1, further comprising said logic circuits for controlling the plurality of column switches and the plurality of row switches that charge adjacent odd and even rows of the pixels with final voltage values representative of the video frame portion represented by the odd row pixels then charge the even rows of the pixels with final voltage values representative of the video frame portion represented by the even row pixels.

14. (original) The system of claim 1, further comprising said logic circuits for controlling the plurality of column switches and the plurality of row switches that charge adjacent odd and even rows of the pixels with final voltage values representative of the video frame portion represented by the even row pixels then charge the odd rows of the pixels with final voltage values representative of the video frame portion represented by the odd row pixels.

15. (original) A method for prewriting a video frame in a liquid crystal display (LCD) having a matrix of liquid crystal pixels, said matrix further divided into a plurality of sub-matrices of pixels, said method comprising the steps of:

calculating average voltage values for each of the sub-matrices of pixels based upon final voltage values for the pixels of each of the sub-matrices;

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writing the calculated average voltage values to the pixels in each of the sub-matrices; and

writing the final voltage values to each of the pixels.

16. (original) The method of claim 15, further comprising the steps of:

storing the pixel final voltage values; and

storing the calculated average voltage values.

17. (original) A method for prewriting a video frame in a liquid crystal display (LCD) having a matrix of liquid crystal pixels arranged in columns and odd and even rows, said matrix further divided into a plurality of sub-matrices of pixels, said method comprising the steps of:

calculating average voltage values for each of the sub-matrices of pixels based upon final voltage values for the pixels of each of the sub-matrices;

writing the calculated average voltage values to the pixels in each of the sub-matrices;

writing the odd row final voltage values to each of the adjacent odd and even rows of pixels; and

writing the even row final voltage values to each of the even rows of pixels.

18. (original) The method of claim 17, further comprising the steps of:

storing the pixel final voltage values; and

storing the calculated average voltage values.

19. (original) A method for prewriting a video frame in a liquid crystal display (LCD) having a matrix of liquid crystal pixels arranged in columns and odd and even rows, said matrix further divided into a plurality of sub-matrices of pixels, said method comprising the steps of:

calculating average voltage values for each of the sub-matrices of pixels based upon final voltage values for the pixels of each of the sub-matrices;

writing the calculated average voltage values to the pixels in each of the sub-matrices;

writing the even row final voltage values to each of the adjacent odd and even rows of pixels; and

writing the odd row final voltage values to each of the odd rows of pixels.

20. (original) The method of claim 19, further comprising the steps of:

storing the pixel final voltage values; and

storing the calculated average voltage values.

21. (previously amended) A liquid crystal display (LCD), comprising:

a matrix of liquid crystal pixels, said matrix further divided into a plurality of sub-matrices of pixels;

at least one digital-to-analog converter (DAC) adapted to receive a digital input representative of an analog voltage and having an analog output adapted for applying the analog voltage to at least one of the pixels at a time;

a plurality of column switches adapted for coupling the analog output of said at least one DAC to at least one of a plurality of columns of said LCD;

a plurality of row switches adapted for selectively coupling the plurality of columns to the pixels of said LCD;

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logic circuits for calculating an average voltage value for each of the plurality of sub-matrices from final voltage values associated with the pixels of each of the sub-matrices; and

logic circuits for controlling the plurality of column switches and the plurality of row switches so that each sub-matrix may be precharged with its calculated average voltage value, then each of the pixels charged with the final voltage value representative of that portion of the video frame represented by that pixel.

22. (original) The LCD of claim 21, wherein the matrix of liquid crystals is K by L, where K and L are positive integer values.

23. (original) The LCD of claim 22, wherein $K > L$.

24. (original) The LCD of claim 22, wherein $K = L$.

25. (original) The LCD of claim 22, wherein $K < L$.

26. (original) The LCD of claim 22, wherein each of the sub-matrices is M by N, wherein M and N are positive integer values, K is greater than or equal to M and L is greater than or equal to N.

27. (original) The LCD of claim 26, wherein M is equal to N.

28. (original) The LCD of claim 26, wherein M is greater than N.

29. (original) The LCD of claim 26, wherein M is less than N.

30. (original) The LCD of claim 22, wherein each of the sub-matrices is M by N, where M and N are positive integer values, and K is greater than or equal to M.

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31. (original) The LCD of claim 22, wherein each of the sub-matrices is M by N, where M and N are positive integer values, and L is greater than or equal to N.

32. (original) The LCD of claim 27, wherein M = N = 8.

33. (original) The LCD of claim 21, further comprising said logic circuits for controlling the plurality of column switches and the plurality of row switches that charge adjacent odd and even rows of the pixels with final voltage values representative of the video frame portion represented by the odd row pixels then charge the even rows of the pixels with final voltage values representative of the video frame portion represented by the even row pixels.

34. (original) The LCD of claim 21, further comprising said logic circuits for controlling the plurality of column switches and the plurality of row switches that charge adjacent odd and even rows of the pixels with final voltage values representative of the video

frame portion represented by the even row pixels then charge the odd rows of the pixels with final voltage values representative of the video frame portion represented by the odd row pixels.

35. (original) The LCD of claim 21, further comprising fabricating the LCD on a semiconductor integrated circuit.

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36. (original) The system of claim 1, further comprising fabricating the LCD system on a semiconductor integrated circuit.